WHAT IS CLAIMED IS:

1. A power source circuit comprising:

a CMOS inversion circuit including a P-channel transistor and an N-channel transistor connected in series between a power source voltage and a reference potential, the transistors being alternately turned "on" or "off" by a PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and being capable of outputting a D.C. voltage to a load via a stabilized capacitance;

a detection circuit outputting a detection signal showing a state where an intermediate node potential at a connection point of the P-channel transistor and the N-channel transistor surpasses the reference potential after undershooting to a level lower than the reference potential when the N-channel transistor is turned "on" during the "off" period of the P-channel transistor;

means for obtaining an error signal by comparing an output from the CMOS inversion circuit with a predetermined reference voltage value; and

means for producing a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the CMOS inversion circuit, controlling the PWM signal supplied to the gate of the N-channel transistor among PWM signals supplied to the CMOS inversion circuit by the detection signal from the detection circuit, and turning "off" an "on" state of the N-channel transistor.

2. The power source circuit claimed in claim 1, wherein the detection circuit comprises:

a first switch being capable of switching the intermediate node potential to the reference potential selectively, and selecting and outputting the intermediate node potential during the "on" period of the N-channel transistor;

a coupling capacitor connected to an output terminal of the first switch in series;

an inverter connected to the output terminal of the coupling capacitor in series, driven by using the same voltage as the power source voltage and the reference potential, inputting and inverting the intermediate node potential during the "on" period of the N-channel transistor, and outputting the intermediate node potential as the detection signal; and

a second switch connected to input and output terminals of the inverter in parallel, being turned "on" during the "on" period of the P-channel transistor, and being turned "off" during the "on" period of the N-channel transistor.

3. A power source circuit comprising:

a CMOS inversion circuit including a P-channel transistor and an N-channel transistor connected in series between a power source voltage and a reference potential, the transistors being alternately turned "on" or "off" by a PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and being capable of outputting D.C. voltage to

a load via a stabilized capacitance;

a detection circuit detecting a zero point position when a potential at a connection point of the P-channel transistor and the N-channel transistor returns to the reference potential after undershooting to a level lower than the reference potential, and outputting a detection signal that shows at least the zero point position when the N-channel transistor is turned "on" during the "off" period of the P-channel transistor;

a current feedback circuit producing a current feedback signal according to a magnitude of a load current based on the detection signal showing the zero point position;

means for obtaining an error signal by comparing the current feedback signal with a predetermined reference voltage value; and

means for producing a PWM signal of which a pulse width is controlled by the error signal, and supplying the PWM signal to each gate of the CMOS inversion circuit.

4. A power source circuit comprising:

a CMOS inversion circuit including a P-channel transistor and an N-channel transistor connected in series between a power source voltage and a reference potential, the transistors being alternately turned "on" or "off" by a PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and being capable of outputting D.C. voltage to a load via a stabilized capacitance;

a detection circuit outputting a first detection signal showing the

state where potential at a connection point of the P-channel transistor and the N-channel transistor surpasses the reference a potential after undershooting to a level lower than the reference potential, at the same time, detecting a zero point position when the potential at the connection point returns to the reference potential after undershooting to the level lower than the reference potential, and outputting a second detection signal that shows at least the zero point position when the N-channel transistor is turned "on" during the "off" period of the P-channel transistor;

a current feedback circuit producing a current feedback signal according to a magnitude of a load current based on the second detection signal showing the zero point position;

means for obtaining an error signal by comparing the current feedback signal with a predetermined reference voltage value; and

means for producing a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the CMOS inversion circuit, at the same time, controlling the PWM signal supplied to the gate of the N-channel transistor among PWM signals supplied to the CMOS inversion circuit by the first detection signal from the detection circuit, and turning "off" an "on" state of the N-channel transistor.

5. A power source circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power source voltage and a reference potential, the transistors being alternately turned "on" or "off" by a

PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and being capable of outputting a D.C. voltage to a load via a stabilized capacitance;

a detection circuit outputting a detection signal showing a state where an intermediate node potential at a connection point of the high side transistor and the low side transistor surpasses the reference potential after undershooting to a level lower than the reference potential when the low side transistor is turned "on" during the "off" period of the high side transistor; and

means for controlling the PWM signal supplied to the gate of the low side transistor among PWM signals supplied to the DC-DC conversion circuit by the detection signal from the detection circuit, and turning "off" an "on" state of the low side transistor.

6. A power source circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power source voltage and a reference potential, turning "on" or "off" the transistors being alternately turned "on" or "off" by a PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and being capable of outputting a D.C. voltage to a load via a stabilized capacitance;

a detection circuit outputting a detection signal showing a state where an intermediate node potential at a connection point of the high side transistor and the low side transistor surpasses the reference potential after

undershooting to a level lower than the reference potential when the low side transistor is turned "on" during the "off" period of the high side transistor;

means for obtaining an error signal by comparing the output from the DC-DC conversion circuit with a predetermined reference voltage value; and

means for producing a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the DC-DC conversion circuit, controlling the PWM signal supplied to the gate of the low side transistor among PWM signals supplied to the DC-DC conversion circuit by the detection signal from the detection circuit, and turning "off" an "on" state of the low side transistor.

7. The power source circuit claimed in claim 5, wherein the detection circuit comprises:

a first switch being capable of switching the intermediate node potential to the reference potential selectively, and selecting and outputting the intermediate node potential during an "on" period of the low side transistor;

a coupling capacitor connected to an output terminal of the first switch in series;

an inverter connected to the output terminal of the coupling capacitor in series, driven by using the same voltage as the power source voltage and the reference potential, inputting and inverting the intermediate node potential during the "on" period of the low side transistor, and

outputting the intermediate node potential as the detection signal; and

a second switch connected to input and output terminals of the inverter in parallel, being turned "on" during the "on" period of the high side transistor, and being turned "off" during the "on" period of the low side transistor.

8. A power source circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power source voltage and a reference potential, turning "on" or "off" the transistors being alternately turned "on" or "off" by a PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and being capable of outputting a D.C. voltage to a load via a stabilized capacitance;

a detection circuit detecting a zero point position when a potential at a connection point of the high side transistor and the low side transistor returns to the reference potential after undershooting to a level lower than the reference potential, and outputting a detection signal that shows at least the zero point position when the low side transistor is turned "on" during the "off" period of the high side transistor;

a current feedback circuit producing a current feedback signal according to a magnitude of a load current based on the detection signal showing the zero point position;

means for obtaining an error signal by comparing the current feedback signal with a predetermined reference voltage value; and

means for producing a PWM signal of which a pulse width is controlled by the error signal, and supplying the PWM signal to each gate of the DC-DC conversion circuit.

9. A power source circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power source voltage and a reference potential, the transistors being alternately turned "on" or "off" by a PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and being capable of outputting a D.C. voltage to a load via a stabilized capacitance;

a detection circuit outputting a first detection signal showing a state where a potential at a connection point of the high side transistor and the low side transistor surpasses the reference potential after undershooting to a level lower than the reference potential, at the same time, detecting a zero point position when the potential at the connection point returns to the reference potential after undershooting to the level lower than the reference potential, and outputting a second detection signal that shows at least the zero point position when the low side transistor is turned "on" during the "off" period of the high side transistor;

a current feedback circuit producing a current feedback signal according to a magnitude of a load current based on the second detection signal showing the zero point position;

means for obtaining an error signal by comparing the current

feedback signal with a predetermined reference voltage value; and

means for producing a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the DC-DC conversion circuit, at the same time, controlling the PWM signal supplied to the gate of the low side transistor among the PWM signals supplied to the DC-DC conversion circuit by the first detection signal from the detection circuit, and turning "off" an "on" state of the low side transistor.

10. The power source circuit claimed according to claim 3, wherein the current feedback circuit implements current feedback by producing the current feedback signal based on the detection signal showing the zero point position only when the magnitude of the load current is larger than a predetermined value.

11. A power source circuit comprising:

a CMOS inversion circuit including a P-channel transistor and an N-channel transistor connected in series between a power source voltage and a reference potential, the transistors being alternately turned "on" or "off" by a PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and being capable of outputting a D.C. voltage to a load via a stabilized capacitance;

a detection circuit outputting a detection signal showing a state where an intermediate node potential at a connection point of the P-channel transistor and the N-channel transistor surpasses the reference potential

after undershooting to a level lower than the reference potential when the N-channel transistor is turned "on" during the "off" period of the P-channel transistor;

an error amplifier that obtains an error signal by comparing an output from the CMOS inversion circuit with a predetermined reference voltage value; and

a PWM circuit and output driver that produce a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the CMOS inversion circuit, controlling the PWM signal supplied to the gate of the N-channel transistor among PWM signals supplied to the CMOS inversion circuit by the detection signal from the detection circuit, and turning "off" an "on" state of the N-channel transistor.

12. The power source circuit claimed in claim 11, wherein the detection circuit comprises:

a first switch being capable of switching the intermediate node potential to the reference potential selectively, and selecting and outputting the intermediate node potential during the "on" period of the N-channel transistor;

a coupling capacitor connected to an output terminal of the first switch in series;

an inverter connected to the output terminal of the coupling capacitor in series, driven by using the same voltage as the power source voltage and the reference potential, inputting and inverting the intermediate

node potential during the "on" period of the N-channel transistor, and outputting the intermediate node potential as the detection signal; and

a second switch connected to input and output terminals of the inverter in parallel, being turned "on" during the "on" period of the P-channel transistor, and being turned "off" during the "on" period of the N-channel transistor.

13. The power source circuit in clam 1 further including a Schottky diode connected between a source and drain of the N-channel transistor.

14. The power source circuit claimed according to claim 4, wherein the current feedback circuit implements current feedback by producing the current feedback signal based on the detection signal showing the zero point position only when the magnitude of the load current is larger than a predetermined value.

15. The power source circuit claimed according to claim 8, wherein the current feedback circuit implements current feedback by producing the current feedback signal based on the detection signal showing the zero point position only when the magnitude of the load current is larger than a predetermined value.

16. The power source circuit claimed according to claim 9, wherein the current feedback circuit implements current feedback by producing the

current feedback signal based on the detection signal showing the zero point position only when the magnitude of the load current is larger than a predetermined value.

17. The power source circuit claimed in claim 11, further comprising a PWM controller that controls the output for the CMOS inversion circuit.

18. The power source circuit claimed in claim 11, wherein the transistors have a common drain.

19. The power source circuit claimed in claim 11, further including a coil and a stabilizing capacitance.

20. The power source circuit claimed in claim 11, further including a schottky diode connected between a source and drain of the N-Channel transistor.